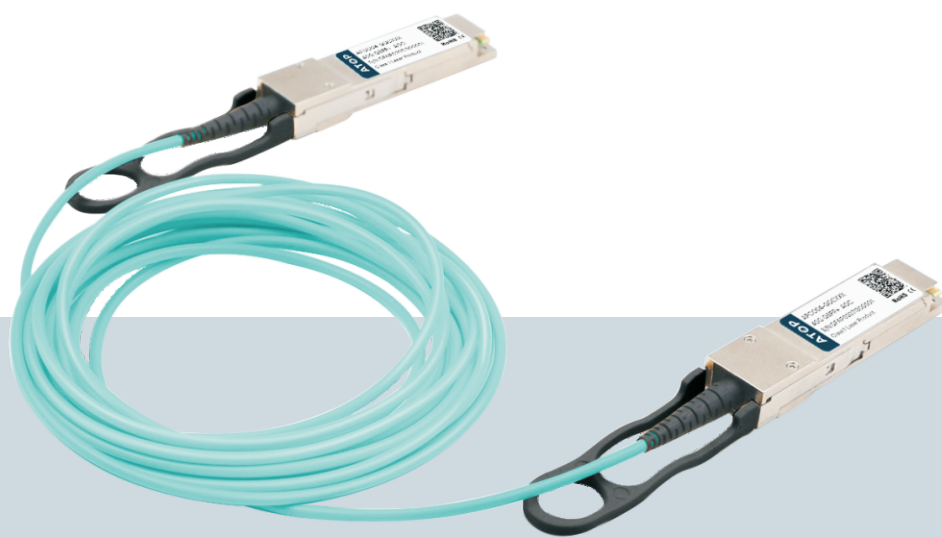




# 40Gb/s QSFP+ Active Optical Cable

APCO04QQCXXX



# 40Gb/s QSFP+ Active Optical Cable

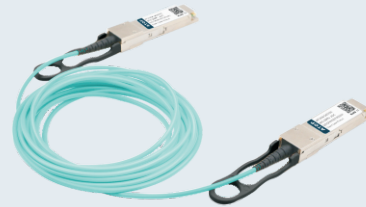
APCO04QQCXXX

## Product Features

- ✓ Available in lengths of 1 to 100m
- ✓ 4 independent full-duplex channels up
- ✓ To 11.3Gbps data rate per wavelength  
Hot-pluggable QSFP +footprint
- ✓ RoHS compliant and Lead Free
- ✓ Power dissipation <1.5W (0~70°C)
- ✓ Commercial operating temperature optional
- ✓ Compliant with IEEE802.3ba, SFF-8436

## Applications

- ✓ 40G Ethernet
- ✓ Infiniband 4X SDR DDR QDR
- ✓ 40G Telecom connections



## Product Selection

| Part Number   | Lengths |
|---------------|---------|
| APCO04-QQC010 | 1m      |
| APCO04-QQC020 | 2m      |
| APCO04-QQC030 | 3m      |
| APCO04-QQC050 | 5m      |
| APCO04-QQC070 | 7m      |
| APCO04-QQC100 | 10m     |
| APCO04-QQC150 | 15m     |
| APCO04-QQC200 | 20m     |
| APCO04-QQC250 | 25m     |
| APCO04-QQC300 | 30m     |
| APCO04-QQC400 | 40m     |
| APCO04-QQC500 | 50m     |
| APCO04-QQC700 | 70m     |
| APCO04-QQCA00 | 100m    |

\*For availability of additional cable lengths, please contact ATOP.

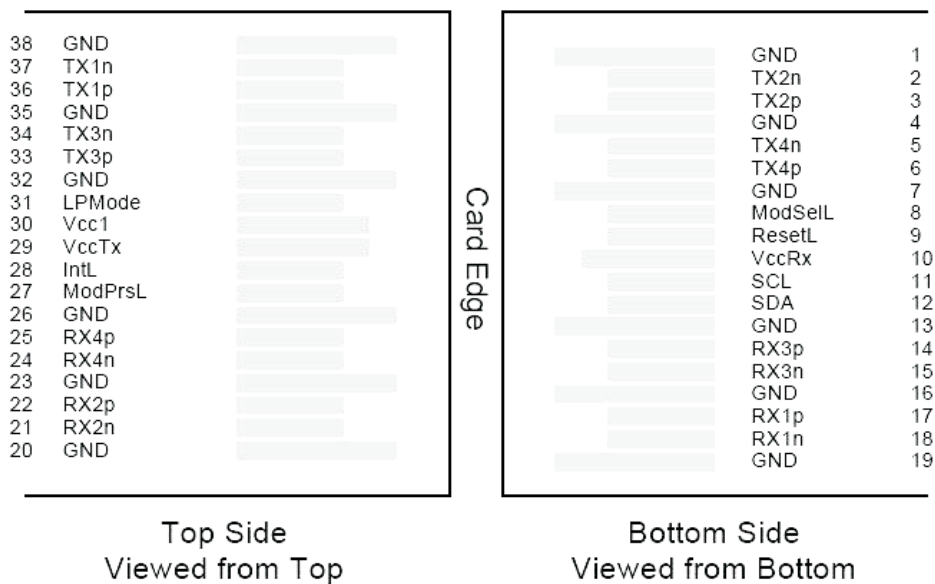
## Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883E Method 3015.7
- Immunity compatible with IEC 61000-4-3
- EMI compatible with FCC Part 15 Class B EN55022 Class B
- ROHS compliant with ROHS 10 (2015/863/EU)

## Pin Descriptions

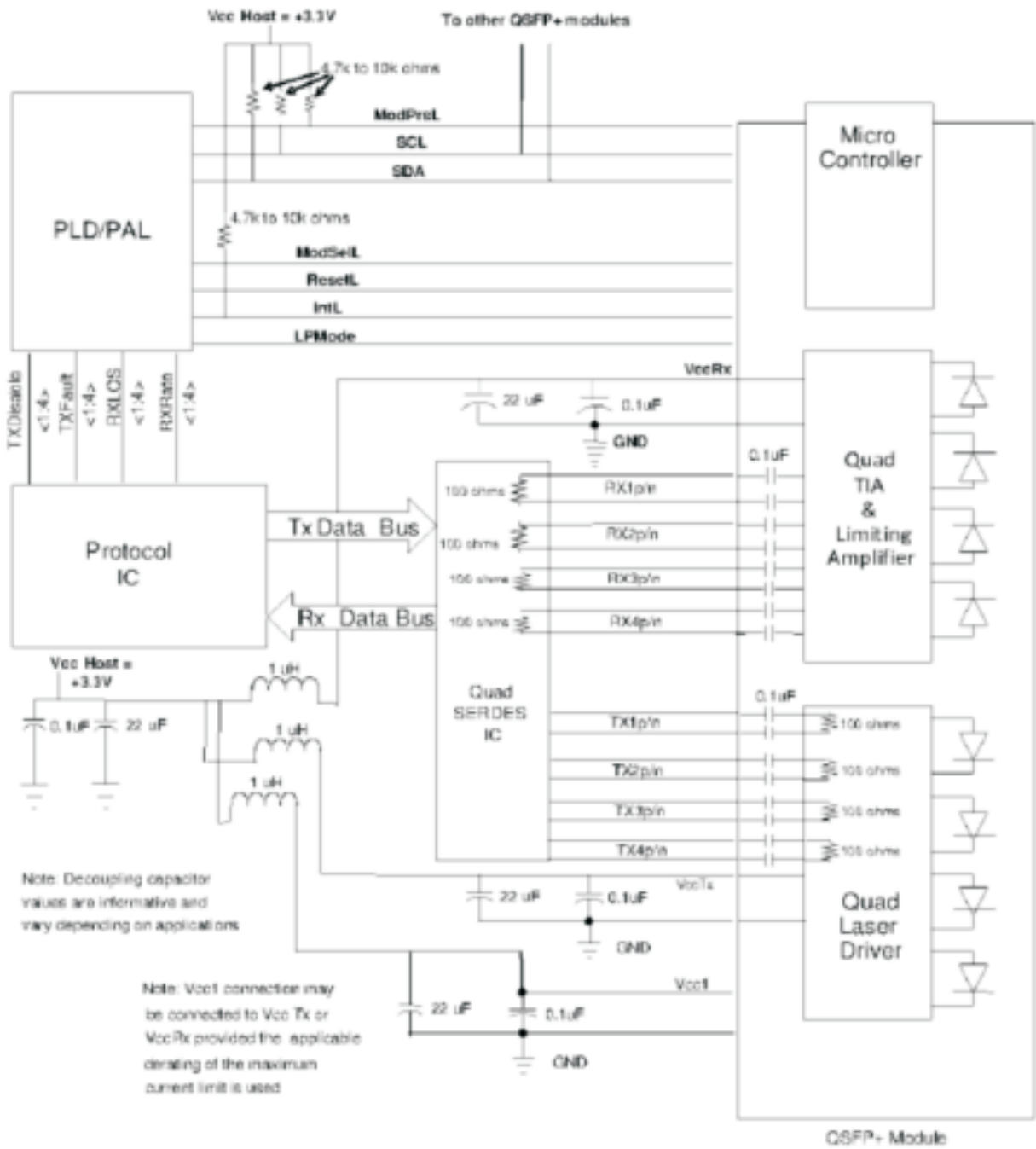
| Pin | Symbol  | Name   | Ref. |
|-----|---------|--|------|
| 1   | GND     | Ground   |      |
| 2   | Tx2n    | Transmitter Inverted Data Input, CML-I   |      |
| 3   | Tx2p    | Transmitter Non-Inverted Data output, CML-I  |      |
| 4   | GND     | Ground   |      |
| 5   | Tx4n    | Transmitter Inverted Data Input, CML-I   |      |
| 6   | Tx4p    | Transmitter Non-Inverted Data output, CML-I  |      |
| 7   | GND     | GND  |      |
| 8   | ModSelL | <p>The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node must be biased to the "High" state in the module</p> |      |
| 9   | ResetL  | <p>The ResetL pin must be pulled to Vcc in the QSFP+ module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released.</p>  |      |
| 10  | VccRx   | + 3.3V Power Supply Receiver   |      |
| 11  | SCL     | 2-Wire Serial Interface Clock  |      |
| 12  | SDA     | 2-Wire Serial Interface Data   |      |
| 13  | GND     | GND  |      |
| 14  | Rx3p    | Receiver Non-Inverted Data Output, CML-O   |      |
| 15  | Rx3n    | Receiver Inverted Data Output, CML-O   |      |
| 16  | GND     | GND  |      |
| 17  | Rx1p    | Receiver Non-Inverted Data Output, CML-O   |      |
| 18  | Rx1n    | Receiver Inverted Data Output, CML-O   |      |
| 19  | GND     | Ground   |      |

|    |         |  |
|----|---------|--|
| 20 | GND     | Ground   |
| 21 | Rx2n    | Receiver Inverted Data Output, CML-O   |
| 22 | Rx2p    | Receiver Non-Inverted Data Output, CML-O   |
| 23 | GND     | Ground   |
| 24 | Rx4n    | Receiver Inverted Data Output, CML-O   |
| 25 | Rx4p    | Receiver Non-Inverted Data Output, CML-O   |
| 26 | GND     | Ground   |
| 27 | ModPrsL | Module Present, connect to GND   |
| 28 | IntL    | The IntL pin is an open collector output and must be pulled to host supply voltage on the host board. The INTL pin is de-asserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read. |
| 29 | VccTx   | +3.3 V Power Supply transmitter  |
| 30 | Vcc1    | +3.3 V Power Supply  |
| 31 | LPMODE  | The LPMODE pin shall be pulled up to Vcc in the QSFP+ module. This function is affected by the LPMODE pin and the combination of the Power_over-ride and Power_set softwarecontrol bits (Address A0h, byte 93 bits 0,1).                                       |
| 32 | GND     | Ground   |
| 33 | Tx3p    | Transmitter Non-Inverted Data Input, CML-I   |
| 34 | Tx3n    | Transmitter Inverted Data Output, CML-I  |
| 35 | GND     | Ground   |
| 36 | Tx1p    | Transmitter Non-Inverted Data Input, CML-I   |
| 37 | Tx1n    | Transmitter Inverted Data Output, CML-I  |
| 38 | GND     | Ground   |



Pin-out of Connector Block on Host Board

Recommend Circuit Schematic



## Absolute Maximum Ratings

| Parameter              | Symbol | Min  | Typ | Max  | Unit | Ref. |
|------------------------|--------|------|-----|------|------|------|
| Maximum Supply Voltage | Vcc    | -0.5 |     | +4.0 | V    |      |
| Storage Temperature    | TS     | -4.0 |     | +85  | °C   |      |
| Operating Humidity     | RH     | 0    |     | 85   | %    |      |

## Recommended Operating Conditions

| Parameter                  | Symbol | Min  | Typ  | Max  | Unit | Ref.       |
|----------------------------|--------|------|------|------|------|------------|
| Power Supply Voltage       | Vcc    | 3.13 | 3.30 | 3.47 | V    |            |
| Power Supply Current       | Icc    | -    | -    | 1    | A    | Commercial |
| Case Operating Temperature | Tc     | 0    | -    | +70  | °C   | Commercial |
| Bit Rate Each Lane         | Br     | 1    | -    | 11.3 | Gbps |            |
| 9/125um G.652 SMF          | Lmax   | -    | -    | 2    | km   |            |

## Electrical Characteristics

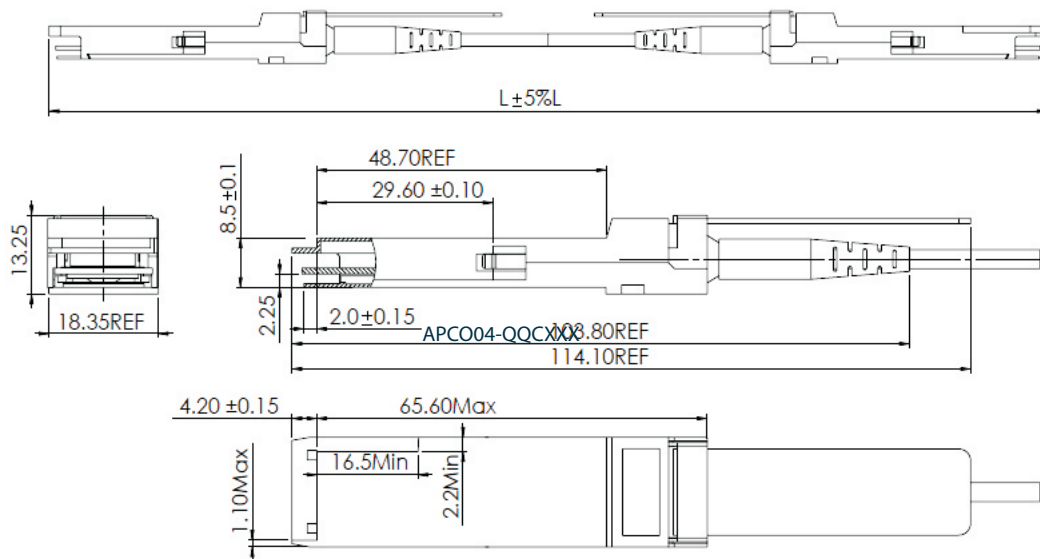
| Parameter                     | Symbol  | Min       | Typ | Max       | Unit | Ref. |
|-------------------------------|---------|-----------|-----|-----------|------|------|
| <b>Transmitter</b>            |         |           |     |           |      |      |
| Input differential impedance  | Rin     | 80        | 100 | 120       | Ω    | 1    |
| Differential data input swing | Vin, pp | 120       | -   | 850       | mV   |      |
| TX Disable-High               | -       | Vcc - 0.8 | -   | Vcc       | V    |      |
| TX Disable-Low                | -       | Vee       | -   | Vee + 0.8 | V    |      |
| TX Fault-High                 | -       | Vcc-0.8   | -   | Vcc       | V    |      |
| TX Fault-Low                  | -       | Vee       | -   | Vee+0.8   | V    |      |

| Parameter                      | Symbol   | Min       | Typ | Max     | Unit | Ref. |
|--------------------------------|----------|-----------|-----|---------|------|------|
| <b>Receiver</b>                |          |           |     |         |      |      |
| Single ended data output swing | Vout, pp | 300       | -   | 850     | mV   | 2    |
| Data output rise time          | Tr       | 30        | -   | -       | ps   | 3    |
| Data output fall time          | Tf       | 30        | -   | -       | ps   | 3    |
| LOS-High                       | -        | Vcc - 0.8 |     | Vcc     | V    |      |
| LOS-Low                        | -        | Vee       |     | Vee+0.8 | V    |      |

Notes:

1. AC coupled.
2. Into 100 ohm differential termination.
3. 20 – 80 %

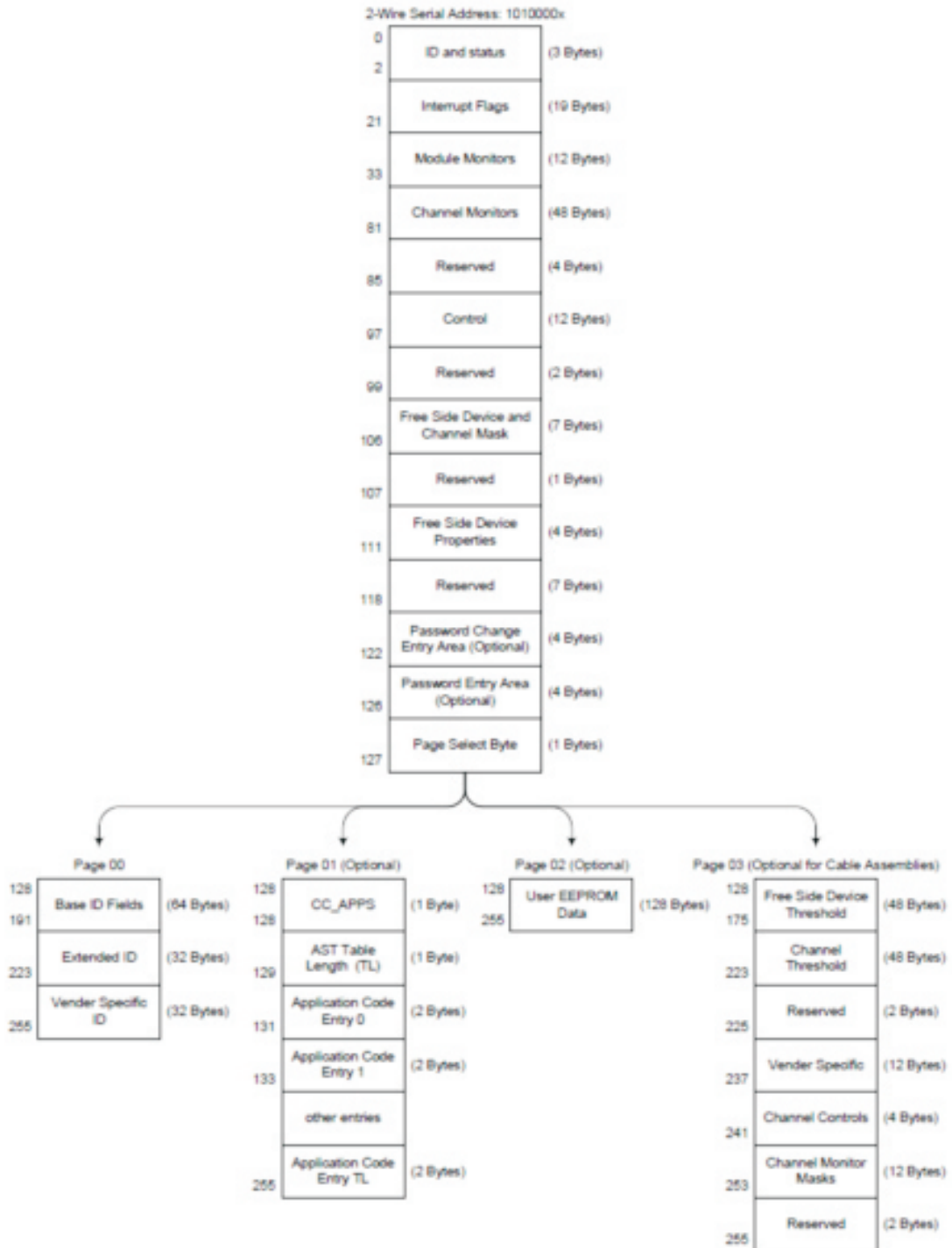
## Mechanical Specifications



APC04-QQCXXX

## EEPROM Information

- EEPROM memory map specific data field description is as below:





## Digital Diagnostic Monitoring Interface

| Parameter    | Range         | Accuracy | Calibration |
|--------------|---------------|----------|-------------|
| Temperature  | 0 to +70°C    | ±3°C     | Internal    |
| Voltage      | 2.97 to 3.63V | ±3%      | Internal    |
| Bias Current | 0 to 100mA    | ±10%     | Internal    |

Four transceiver parameter values are monitored. The following table defines the Monitor parameter's accuracy.

## Revision History

| Revision   | Initiated    | Reviewed     | Approved  | DCN                     | Release Date |
|------------|--------------|--------------|-----------|-------------------------|--------------|
| Version1.0 | Cade.chen    | Tangzhiqiang | dingzheng | New Released.           | Sep 11, 2017 |
| Version1.1 | Tangzhiqiang | Litao        | dingzheng | Update the new template | Dec 19, 2019 |



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