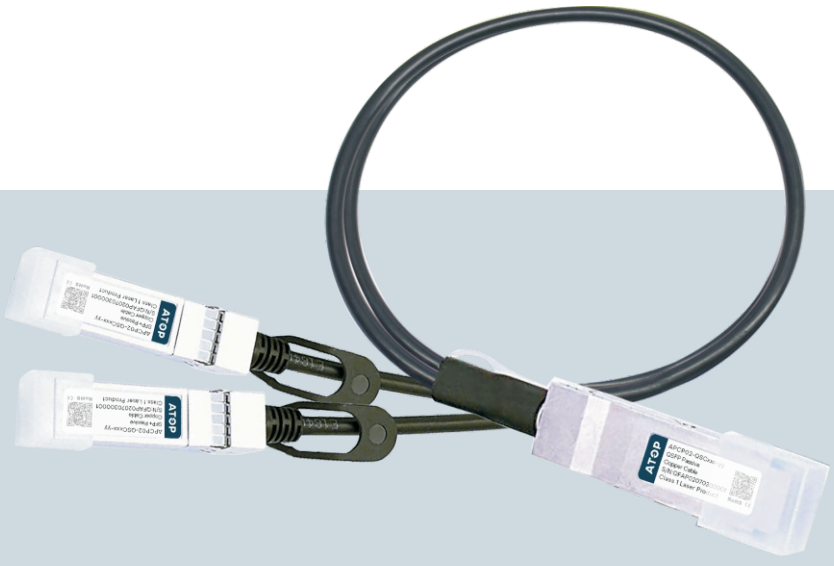
QSFP+ to 2xSFP+ Passive Cable

APCP02-QSCxxx-yy



QSFP+ to 2xSFP+ Passive Cable

APCP02-QSCxxx-yy

The cables are compliant with InfiniBand Architecture, SFF-8436 specifications and provide connectivity between devices using QSFP ports. The QSFP cable is an assembly of 4 full-duplex lanes, where each lane is capable of transmitting data at rates up to 10Gb/s per direction, providing an aggregated rate of 40Gb/s. SFP+ (Small Form-Factor Pluggable)Interconnect System supports next-generation speeds of standard SFP applications, rates up to 10.0Gbps, Application in 10G Ethernet, fiber channel 8G and InfiniBand short interconnection scenarios, Can meet the hardware communication equipment and data center under the request of low cost, low power consumption to achieve the high density port configuration. Conform to the MSA SFF-8431&8431, EMI standard requirements.
QSFP 40 g + To 2 x10g SFP + support two kinds of interface equipment interconnection, single channel transfer rate of 10 GBPS.

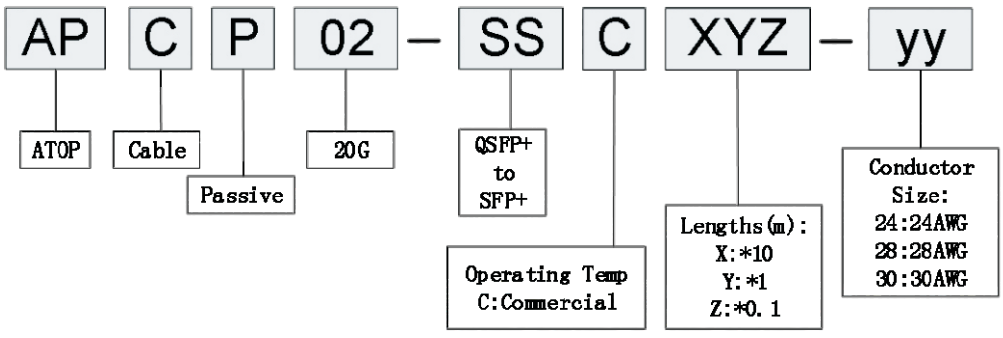
Product Features

- ✓ Compliant with SFF-8436，SFF-8431
- ✓ Compliant with IEEE802.3ba
- ✓ 12C based two-wire serial interface for easy control and monitoring
  All-metal housing for superior EMI performance
- ✓ Low crosstalk
- ✓ Low power consumption
- ✓ RoHS compliant

Applications

- ✓ Data Server
- ✓ Networked storage systems
- ✓ Router
- ✓ External storage system
- ✓ Data Center networking
- ✓ Communications Switches
- ✓ Routers

Product Selection



Part Number	Lengths	Conductor Size	Note
APCP02-QSC005-yy	0.5m	24/26/28/30 AWG	1,2
APCP02-QSC010-yy	1m	24/26/28/30 AWG	1,2
APCP02-QSC015-yy	1.5m	24/26/28/30 AWG	1,2
APCP02-QSC020-yy	2m	24/26/28/30 AWG	1,2
APCP02-QSC025-yy	2.5m	24/26/28/30 AWG	1,2
APCP02-QSC030-yy	3m	24/26/28/30 AWG	1,2
APCP02-QSC050-yy	5m	24/26/28/30 AWG	1,2
APCP02-QSC070-yy	7m	24/26/28/30 AWG	1,2

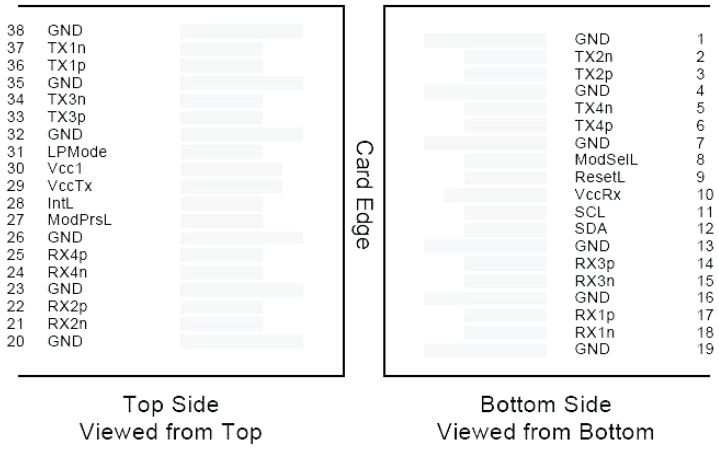
Note:
1, yy=30,28,26,24, present wire size AWG
2, 24 AWG is default

Pin Descriptions

QSFP+ End

Pin	Symbol	Name	Ref.
1	GND	Ground	
2	Tx2n	Transmitter Inverted Data Input, CML-I	
3	Tx2p	Transmitter Non-Inverted Data output, CML-I	
4	GND	Ground	
5	Tx4n	Transmitter Inverted Data Input, CML-I	
6	Tx4p	Transmitter Non-Inverted Data output, CML-I	
7	GND	GND	
8	ModSelL	The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on asingle 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node must be biased to the "High" state in the module	
9	ResetL	The ResetL pin must be pulled to Vcc in the QSFP+ module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released.	
10	VccRx	+ 3.3V Power Supply Receiver	
11	SCL	2-Wire Serial Interface Clock	

12	SDA	2-Wire Serial Interface Data
13	GND	GND
14	Rx3p	Receiver Non-Inverted Data Output, CML-O
15	Rx3n	Receiver Inverted Data Output, CML-O
16	GND	GND
17	Rx1p	Receiver Non-Inverted Data Output, CML-O
18	Rx1n	Receiver Inverted Data Output, CML-O
19	GND	Ground
20	GND	Ground
21	Rx2n	Receiver Inverted Data Output, CML-O
22	Rx2p	Receiver Non-Inverted Data Output, CML-O
23	GND	Ground
24	Rx4n	Receiver Inverted Data Output, CML-O
25	Rx4p	Receiver Non-Inverted Data Output, CML-O
26	GND	Ground
27	ModPrsL	Module Present, connect to GND
28	IntL	The IntL pin is an open collector output and must be pulled to host supply voltage on the host board. The INTL pin is de-asserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read.
29	VccTx	+3.3 V Power Supply transmitter
30	Vcc1	+3.3 V Power Supply
31	LPMode	The LPMode pin shall be pulled up to Vcc in the QSFP+ module. This function is affected by the LPMode pin and the combination of the Power_over-ride and Power_set softwarecontrol bits (Address A0h, byte 93 bits 0,1).
32	GND	Ground
33	Tx3p	Transmitter Non-Inverted Data Input, CML-I
34	Tx3n	Transmitter Inverted Data Output, CML-I
35	GND	Ground
36	Tx1p	Transmitter Non-Inverted Data Input, CML-I
37	Tx1n	Transmitter Inverted Data Output, CML-I
38	GND	Ground



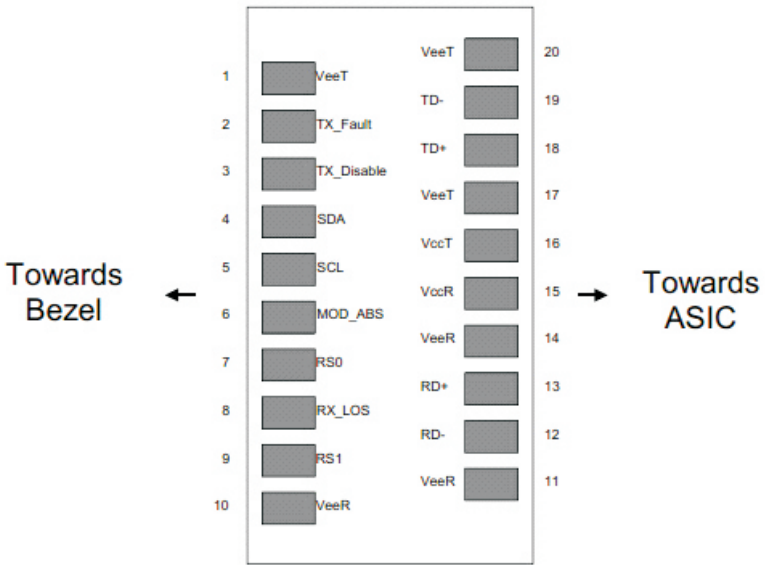
Pin-out of Connector Block on Host Board

SFP+ End

Pin	Symbol	Name	Ref.
1	VeeT	Transmitter Ground (Common with Receiver Ground)	1
2	TX Fault	Transmitter Fault. LVTTL-O	2
3	TX Disable	Transmitter Disable. Laser output disabled on high or open. LVTTL-I	3
4	SDA	2-Wire Serial Interface Data Line (Same as MOD-DEF2 in INF-8074i). LVTTL-I/O	2
5	SCL	2-Wire Serial Interface Data Line (Same as MOD-DEF2 in INF-8074i). LVTTL-I	2
6	Mod_ABS	Module Absent, Connect to VeeT or VeeR in Module.	2
7	RS0	Rate Select 0, optionally controls SFP+ module receiver LVTTL-I	4
8	LOS	Loss of Signal indication. Logic 0 indicates normal operation. LVTTL-O	5
9	RS1	Rate Select 1, optionally controls SFP+ module transmitter. LVTTL-I	4
10	VeeR	Receiver Ground (Common with Transmitter Ground)	1
11	VeeR	Receiver Ground (Common with Transmitter Ground)	1
12	RD-	Receiver Inverted DATA out. AC Coupled. CML-O	
13	RD+	Receiver Non-inverted DATA out. AC Coupled. CML-O	
14	VeeR	Receiver Ground (Common with Transmitter Ground)	1
15	VccR	Receiver Power Supply	6
16	VccT	Transmitter Power Supply	6
17	VeeT	Transmitter Ground (Common with Receiver Ground)	1
18	TD+	Transmitter Non-Inverted DATA in. AC Coupled. CML- I	
19	TD-	Transmitter Inverted DATA in. AC Coupled. CML- I	
20	VeeT	Transmitter Ground (Common with Receiver Ground)	1

Notes:

1. Circuit ground is internally isolated from chassis ground.
2. T_fault is an open collector/drain output. Which should be pulled up with a 4.7K – 10K Ohms resistor on the host board if intended for use. Pull up voltage should be between 2.0V to Vcc+0.3V.A high output indicates a transmitter fault caused by either the tx bias current or the tx output power exceeding the preset alarm thresholds.A low output indicates normal operation. IN the low state, the output is pulled to <0.8V.
3. Laser output disabled on TX Disable >2.0V or open, enabled on TX Disable<0.8V.
4. Internally pulled down per SFF-8431 Rev4.1 .
5. LOS is open collector output. Should be pulled up with 4.7k – 10kohms on host board to a voltage between 2.0V and 3.6V. Logic 0 indicates normal operation; logic 1 indicates loss of signal.
6. Internally connected



Pin-out of Connector Block on Host Board

Signal Integrity

ITEM		REQUIREMENT	TEST CONDITION
Differential Impedance	Cable Impedance	105+5/-5Ω	Rise time of 35ps (20 % - 80 %).
	Paddle Card Impedance	100±10Ω	
	Cable Termination Impedance	100±15Ω	
[Differential (Input/Output) Return loss S_{DD11}/S_{DD22}]		Return loss(f) ≥ 10 (0.01≤f < 4.1); 6.3-13log10(f/ 5.5) (4.1≤f≤11.1) Where f is the frequency in GHz Return loss(f) is the return loss at frequency f	0.01GHz≤f≤11.1GHz SFF-8431 Rev.4.1

(Differential Insertion Loss Max.)

Differential Insertion Loss (S_{DD21} Max.)	F / AWG	600MHz	1.25GHz	2.5GHz	5.0GHz	0.01GHz≤f≤11.1GHz
	30(1m)Max	2dB	3dB	4.5dB	7.5dB	
	30(2m)Max	4dB	5dB	7dB	10dB	
	30(3m)Max	4dB	5.5dB	7.5 dB	12dB	
	26(5m)Max	5.5dB	7dB	10dB	16.0dB	
	24(7&10m)Max	6.5dB	10dB	14dB	21dB	
MDNEXT(multiple disturber near-end crosstalk)	≥26dB @5GHz					0.01GHz≤f≤11.1GHz
Insertion Loss Deviation	-0.7-0.2*10-3f ≤ ILD ≤ 0.7+0.2*10-3f (f is the frequency in MHz)					0.01GHz≤f≤5.0GHz

Other Electrical Performance

ITEM	REQUIREMENT	TEST CONDITION
Low Level Contact Resistance	70milliohms Max. From initial.	EIA-364-23:Apply a maximum voltage of 20mV And a current of 100 mA.
Insulation Resistance	10Mohm(Min.)	EIA364-21:AC 300V 1minute
Dielectric Withstanding Voltage	DC 500V 1 minute disruptive discharge.	EIA-364-20:Apply a voltageof 500 VDC for 1minute between adjacent terminals And between adjacent terminals and ground.

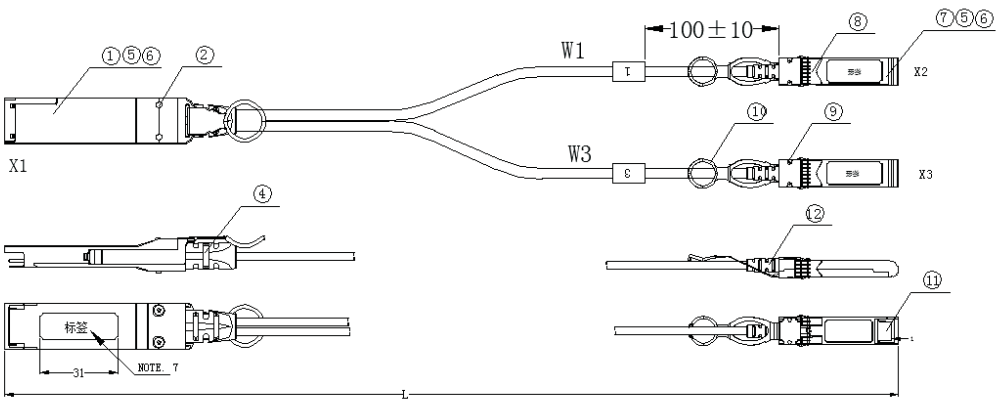
Environment Performance

ITEM	REQUIREMENT	TEST CONDITION
Operating Temp. Range	0°C to +70°C	Cable operating temperature range.
Storage Temp. Range (in packed condition)	-40°C to +80°C	Cable storage temperature range in packed condition.
Thermal Cycling Non-Powered	No evidence of physical damage	EIA-364-32D, Method A, -25 to 90C, 100 cycles, 15 min. dwells
Salt Spraying	48 hours salt spraying after shell corrosive area less than 5%.	EIA-364-26
Mixed Flowing Gas	Pass electrical tests per 3.1 after stressing. (For connector only)	EIA-364-35 Class II,14 days.
Temp. Life	No evidence of physical damage	EIA-364-17C w/ RH, Damp heat 90℃ at 85% RH for 500 hours then return to ambient
Cable Cold Bend	4H, No evidence of physical damage	Condition: -20℃±2℃, mandrel diameter is 6 times the cable diameter.

Mechanical and Physical Characteristics

ITEM	REQUIREMENT	TEST CONDITION
Vibration	Pass electrical tests per 3.1 after stressing.	Clamp & vibrate per EIA-364-28E,TC-VII, test condition letter – D, 15 minutes in X, Y & Z axis.
Cable Flex	No evidence of physical damage	Flex cable 180° for 20 cycles (±90° from nominal position) at 12 cycles per minute with a 1.0kg load applied to the cable jacket. Flex in the boot area 90º in each direction from vertical. Per EIA-364-41C
Cable Plug Retention in Cage	90N Min. No evidence of physical damage	Pull on cable jacket approximately 1 ft behind cable plug. No functional damage to cable plug below 90N. Per SFF-8432 Rev 5.0
Cable Retention in Plug	90N Min. No evidence of physical damage	Cable plug is fixtured with the bulk cable hanging vertically. A 90N axial load is applied (gradually) to the cable jacket and held for 1 minute. Per EIA-364-38B
Mechanical Shock	Pass electrical tests Per 3.1 after stressing.	Clamp and shock per EIA-364-27B, TC-G,3 times in 6 directions, 100g, 6ms.
Cable Plug Insertion	40N Max. (QSFP+) 18N Max. (SFP+)	Per SFF-8432 Rev 5.0
Cable plug Extraction	30N Max. (QSFP28) 12.5N Max. (SFP28)	Measure without the aid of any cage kick-out springs. Place axial load on de-latch to de-latch plug. Per SFF-8432 Rev 5.0
Durability	50 cycles, No evidence of physical damage	EIA-364-09, perform plug &unplug cycles: Plug and receptacle mate rate: 250times/hour. 50times for module (CONNECTOR TO PCB)

Mechanical Specifications



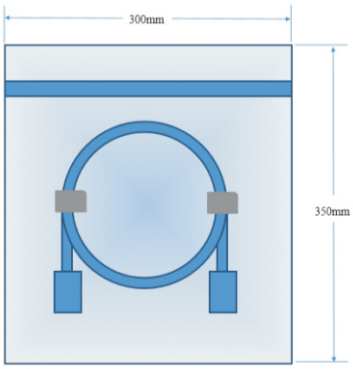
Wiring Diagram

wire	Starting signal	Starting	End	End signal
W1	RX1+	X1.17	X2.18	TX1+
	RX1-	X1.18	X2.19	TX1-
	GND	X1.19	X2.20	GND
	TX1+	X1.36	X2.13	RX1+
	TX1-	X1.37	X2.12	RX1-
	GND	X1.38	X2.14	GND

wire	Starting signal	Starting	End	End signal
W3	RX3+	X1.14	X3.18	TX3+
	RX3-	X1.15	X3.19	TX3-
	GND	X1.16	X3.20	GND
	TX3+	X1.33	X3.13	RX3+
	TX3-	X1.34	X3.12	RX3-
	GND	X1.35	X4.14	GND

Package diagram

<=3m: 200mm*300mm
>3m: 300mm*350mm



Revision History

Revision	Initiated	Reviewed	Approved	DCN	Release Date
Version1.0	Tangzhiqiang	Li Tao	Ding zheng	New Released.	Nov 19, 2019

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