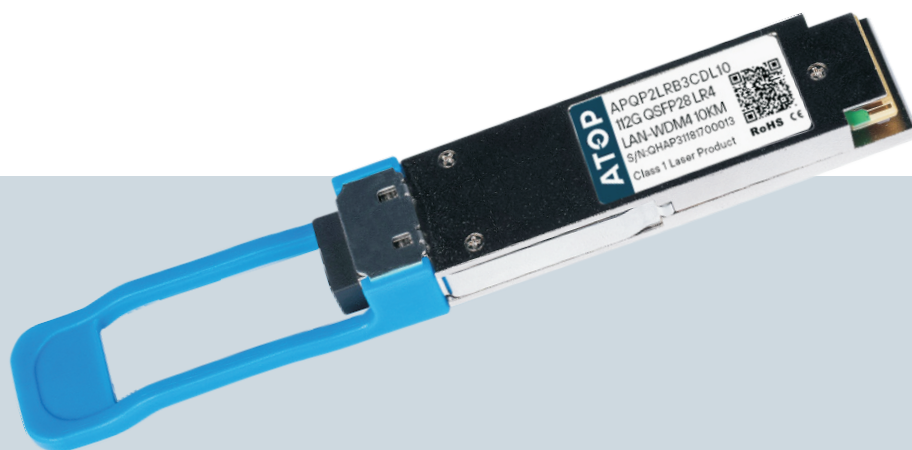




112/103Gb/s QSFP28 LR4 Transceiver

APQP2LRB3CDL10



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Product Features

- ✓ 4 LAN-WDM lanes MUX/DEMUX design
- ✓ 4 independent full-duplex channels up To 28Gbps data rate per wavelength
- ✓ Hot-pluggable QSFP28 footprint
- ✓ RoHS compliant and Lead Free
- ✓ Up to 10km link length
- ✓ Power dissipation <4.5W (0~70°C)
- ✓ Commercial operating temperature optional

Applications

- ✓ 100GBASE-LR4
- ✓ 100GEthernet
- ✓ OTU4 4I1-9D1F



Product Selection

| Part Number | Operating Case temperature | DDMI |
|----------------|----------------------------|------|
| APQP2LRB3CDL10 | Commercial(0~70°C) | Yes |

Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883 Method 3015
- ESD to the Duplex LC Receptacle: compatible with EN 61000-4-2
- Immunity compatible with EN 61000-4-3
- EMI compatible with FCC Part 15 Class B
- Laser Eye Safety compatible with FDA 21CFR 1040.10 and 1040.11 IEC 60950, IEC60825-1,2
- RoHS compliant with RoHS 2.0(2015/863/EU)-amending.

Pin Descriptions

| Pin | Symbol | Name | Ref. |
|-----|---------|--|------|
| 1 | GND | Ground | |
| 2 | Tx2n | Transmitter Inverted Data Input, CML-I | |
| 3 | Tx2p | Transmitter Non-Inverted Data output, CML-I | |
| 4 | GND | Ground | |
| 5 | Tx4n | Transmitter Inverted Data Input, CML-I | |
| 6 | Tx4p | Transmitter Non-Inverted Data output, CML-I | |
| 7 | GND | GND | |
| 8 | ModSelL | <p>The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node must be biased to the "High" state in the module</p> | |
| 9 | ResetL | <p>The ResetL pin must be pulled to Vcc in the QSFP+ module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released.</p> | |
| 10 | VccRx | + 3.3V Power Supply Receiver | |
| 11 | SCL | 2-Wire Serial Interface Clock | |
| 12 | SDA | 2-Wire Serial Interface Data | |
| 13 | GND | GND | |
| 14 | Rx3p | Receiver Non-Inverted Data Output, CML-O | |
| 15 | Rx3n | Receiver Inverted Data Output, CML-O | |
| 16 | GND | GND | |
| 17 | Rx1p | Receiver Non-Inverted Data Output, CML-O | |
| 18 | Rx1n | Receiver Inverted Data Output, CML-O | |
| 19 | GND | Ground | |
| 20 | GND | Ground | |
| 21 | Rx2n | Receiver Inverted Data Output, CML-O | |
| 22 | Rx2p | Receiver Non-Inverted Data Output, CML-O | |
| 23 | GND | Ground | |
| 24 | Rx4n | Receiver Inverted Data Output, CML-O | |
| 25 | Rx4p | Receiver Non-Inverted Data Output, CML-O | |
| 26 | GND | Ground | |
| 27 | ModPrsL | Module Present, connect to GND | |

| Pin | Symbol | Name | Ref. |
|-----|--------|--|------|
| 28 | IntL | The IntL pin is an open collector output and must be pulled to host supply voltage on the host board. The INTL pin is de-asserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read. | |
| 29 | VccTx | +3.3 V Power Supply transmitter | |
| 30 | Vcc1 | +3.3 V Power Supply | |
| 31 | LPMoDe | The LPMoDe pin shall be pulled up to Vcc in the QSFP+ module. This function is affected by the LPMoDe pin and the combination of the Power_over-ride and Power_set softwarecontrol bits (Address A0h, byte 93 bits 0,1). | |
| 32 | GND | Ground | |
| 33 | Tx3p | Transmitter Non-Inverted Data Input, CML-I | |
| 34 | Tx3n | Transmitter Inverted Data Output, CML-I | |
| 35 | GND | Ground | |
| 36 | Tx1p | Transmitter Non-Inverted Data Input, CML-I | |
| 37 | Tx1n | Transmitter Inverted Data Output, CML-I | |
| 38 | GND | Ground | |

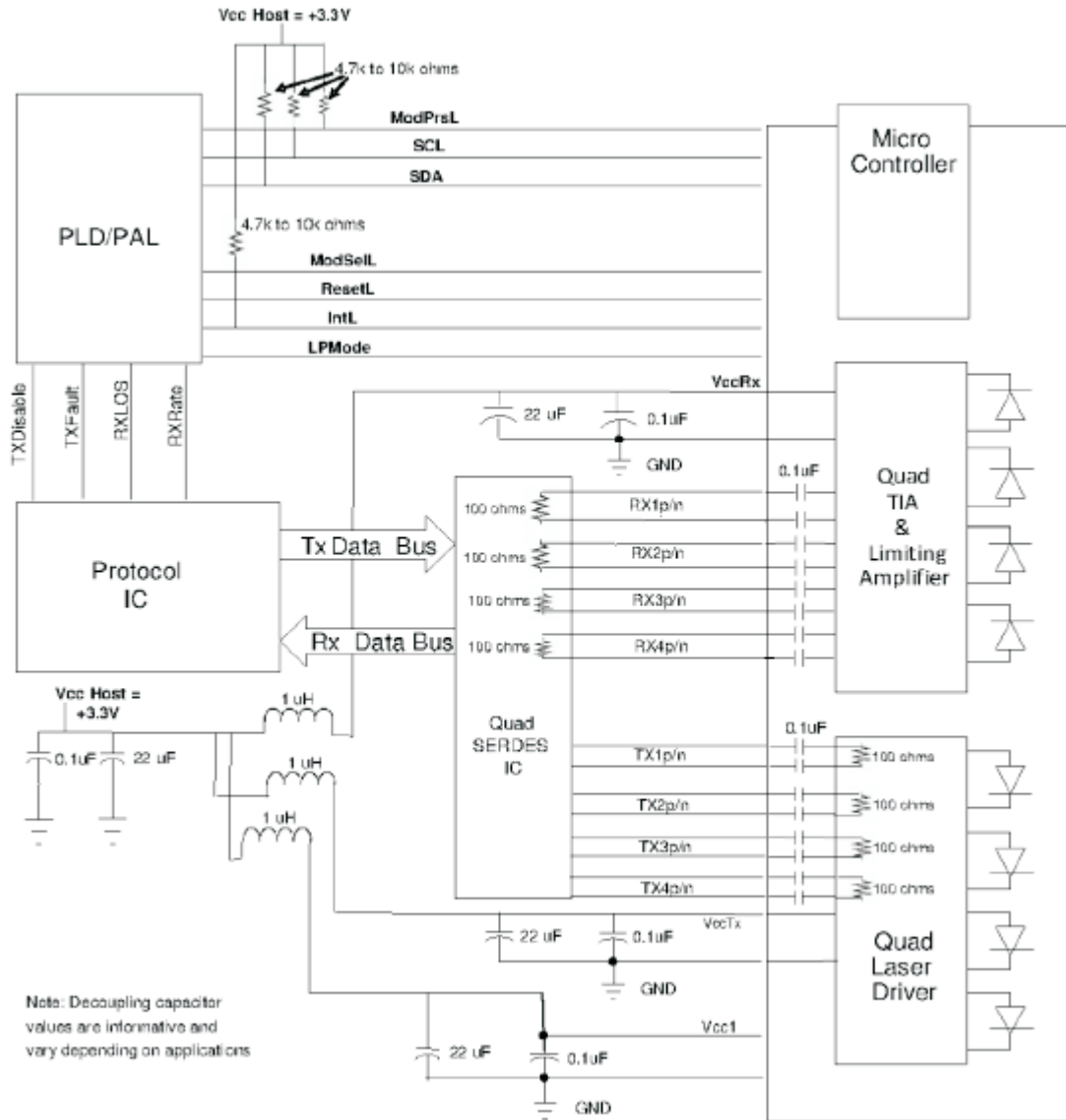


Top Side
Viewed from Top

Bottom Side
Viewed from Bottom

Pin-out of Connector Block on Host Board

Recommend Circuit Schematic



Absolute Maximum Ratings

| Parameter | Symbol | Min | Typ | Max | Unit | Ref. |
|------------------------|--------|------|-----|------|------|------|
| Maximum Supply Voltage | Vcc | -0.5 | | +4.0 | V | |
| Storage Temperature | TS | -40 | | +85 | °C | |
| Operating Humidity | RH | 0 | | 85 | % | |

Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit | Ref. |
|----------------------------|--------|------|------|------|------|------------|
| Power Supply Voltage | Vcc | 3.13 | 3.30 | 3.47 | V | |
| Power Supply Current | Icc | - | - | 1.29 | A | Commercial |
| Case Operating Temperature | Tc | 0 | | +70 | °C | Commercial |
| Bit Rate Each Lane | Br | | - | 28 | Gbps | |
| 9/125um G.652 SMF | Lmax | - | - | 10 | km | |

Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Ref. |
|--------------------------------|-----------------------|----------------------|-----|----------------------|------|------|
| Transmitter | | | | | | |
| Input differential impedance | Rin | 90 | 100 | 110 | Ω | 1 |
| Differential data input swing | V _{in} , pp | 95 | - | 900 | mV | |
| TX Disable-High | - | V _{cc} -0.8 | - | V _{cc} | V | |
| TX Disable-Low | - | V _{ee} | - | V _{ee} +0.8 | V | |
| TX Fault-High | - | V _{cc} -0.8 | - | V _{cc} | V | |
| TX Fault-Low | - | V _{ee} | - | V _{ee} +0.8 | V | |
| Receiver | | | | | | |
| Output differential impedance | Rin | 90 | 100 | 110 | Ω | 1 |
| Single ended data output swing | V _{out} , pp | - | - | 900 | mV | 2 |
| LOS-High | - | V _{cc} -0.8 | | V _{cc} | V | |
| LOS-Low | - | V _{ee} | | V _{ee} +0.8 | V | |

Notes:

1. AC coupled.
2. Into 100 ohm differential termination.

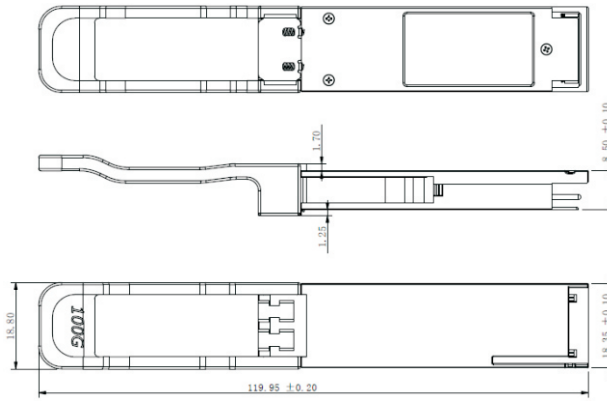
Optical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Ref. |
|--|--------------|----------------------------------|---------|---------|------|------|
| Transmitter | | | | | | |
| Optical Wavelength | L0 | 1294.53 | 1295.56 | 1296.59 | nm | |
| | L1 | 1299.02 | 1300.05 | 1301.09 | nm | |
| | L2 | 1303.54 | 1304.58 | 1305.63 | nm | |
| | L3 | 1308.09 | 1309.14 | 1310.19 | nm | |
| Side-mode Suppression Ratio | SMSR | 30 | | | dB | |
| Total Average Launch Power | PT | | | 10.5 | dBm | |
| Average Launch Power @25.78Gb/s, each Lane | | -4.3 | | +4.5 | dBm | |
| Optical Modulation Amplitude @25.78 Gb/s, each Lane | OMA | -1.3 | | +4.5 | dBm | |
| Average Launch Power @27.95Gb/s, each Lane | | -0.6 | | +4.0 | dBm | |
| Difference in Launch Power Between any Two Lanes (OMA) | P_{Δ} | | | 5 | dB | |
| OMA-TDP @25.78Gb/s, each Lane | OMA-TDP | -2.3 | | | dBm | |
| Extinction Ratio | ER | 4 | | | dB | |
| Transmitter and Dispersion Penalty @25.78Gb/s, each Lane | TDP | | | 2.2 | dB | |
| Transmitter and Dispersion Penalty @27.95Gb/s, each Lane | TDP | | | 1.5 | dB | |
| Optical Eye Mask, 100GE | | Compliant with IEEE 802.3ba-2010 | | | | |
| Optical Eye Mask, OTU4 | | Compliant with ITU-T G.695 | | | | |
| Receiver | | | | | | |
| RX Sensitivity @25.78Gb/s, each lane | SENS | | | -8.6 | dBm | 1 |
| RX Sensitivity @27.95Gb/s, each lane | SENS | | | -8.4 | dBm | 2 |
| Receiver Overload @25.78Gb/s | | 4.5 | | | dBm | |
| Receiver Overload @27.95Gb/s | | 2.9 | | | dBm | |
| LOS De-Assert | LOSD | | | -12 | dBm | |
| LOS Assert | LOSA | -25 | | | dBm | |
| LOS Hysteresis | | 0.5 | | | dB | |

Notes:

- 1.Measured with PRBS 2³¹-1 at 1E-12 BER.
- 2.Measured with PRBS 2³¹-1 at 1E-6 BER.

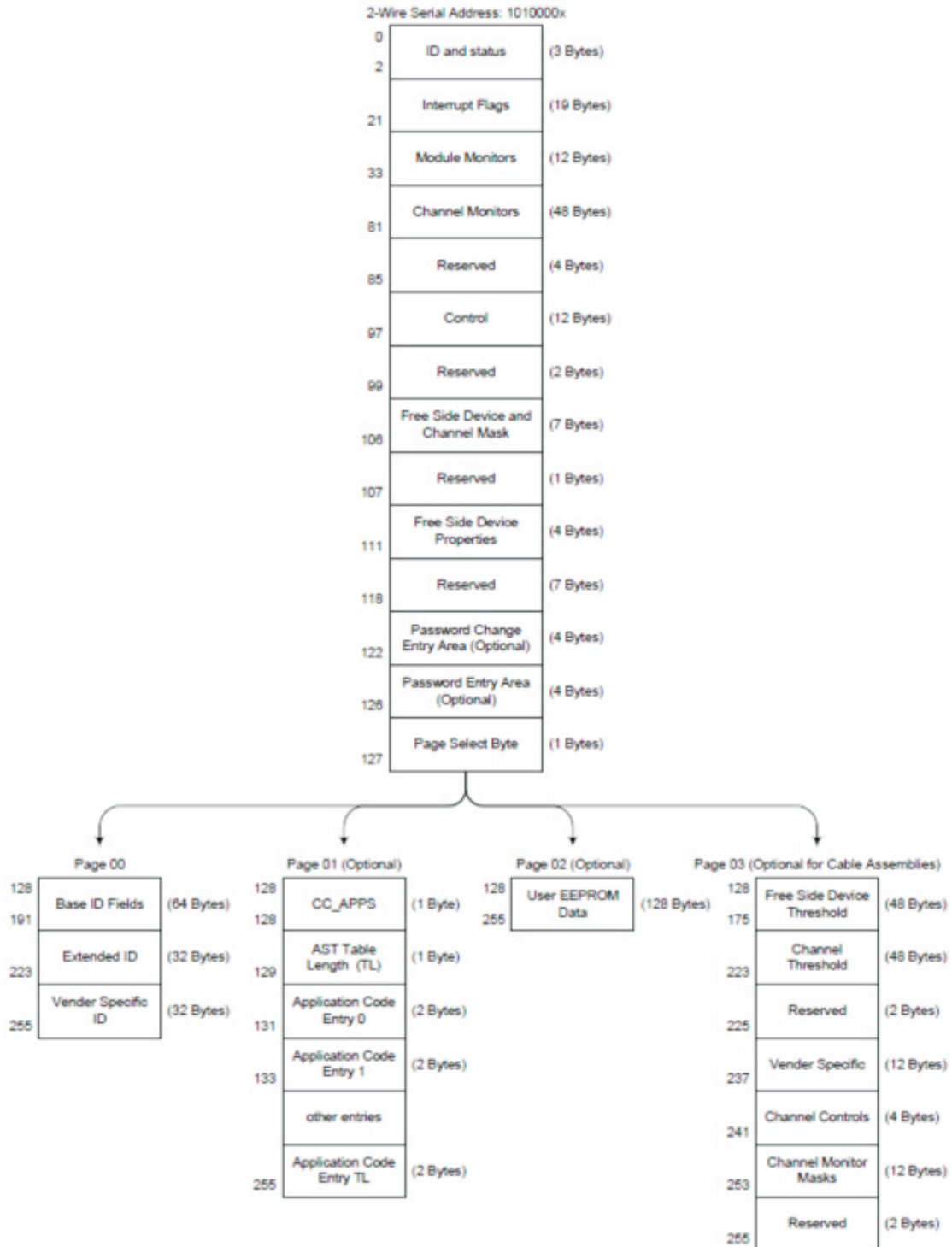
Mechanical Specifications



APQP2LRB3CDL10

EEPROM Information

- EEPROM memory map specific data field description is as below:



Digital Diagnostic Monitoring Interface

Four transceiver parameter values are monitored. The following table defines the monitoring parameter's accuracy.

| Parameter | Range | Accuracy | Calibration |
|--------------|----------------|----------|-------------|
| Temperature | 0 to +70°C | ±3°C | Internal |
| Voltage | 2.97 to 3.63V | ±3% | Internal |
| Bias Current | 0 to 100mA | ±10% | Internal |
| RX Power | -8.6 to 4.5dBm | ±3dB | Internal |

Revision History

| Revision | Initiated | Reviewed | Approved | DCN | Release Date |
|------------|-------------|-------------|-----------|---|----------------|
| Version1.0 | Colin Huang | Billy Tang | Dingzheng | New Released. | Apr 29, 2019 |
| Version1.1 | Colin Huang | Billy Tang | Dingzheng | OTU4 SEN spec update add the TDP spec | Jan17, 2020 |
| Version1.2 | Billy Tang | Colin Huang | Dingzheng | Update the new template | April 10, 2020 |
| Version1.3 | Tang Rong | Billy Tang | Yuan Wei | 1.Add Transmitter eye mask definition. 2.Update Receiver Sensitivity @25.78Gb/s. 3.Update power supply current is 1.29A. | Mar 19, 2021 |



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