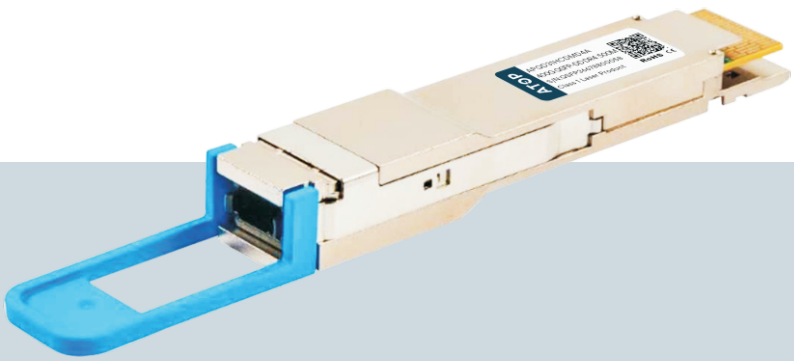
400Gb/s QSFP-DD DR4 Transceiver

APQD31HCDMD4A



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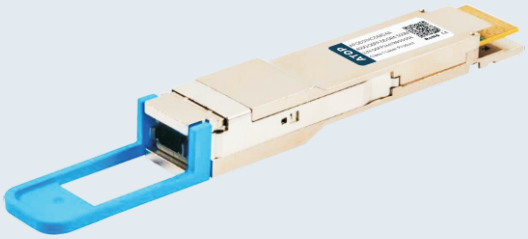
Product Features

- ✓ QSFP-DD MSA compliant
- ✓ Compliant to 802.3bs
- ✓ 400G DR4 Specification compliant
- ✓ Non-hermetic package design
- ✓ 8x53.125Gb/s PAM4 electrical interface (400GAUI-8)
- ✓ Maximum power consumption 12W
- ✓ MPO connector
- ✓ Supports 425Gb/s aggregate bit rate
- ✓ Up to 500m transmission on single mode fiber with FEC
- ✓ Operating case temperature: 0~+70℃
- ✓ Single 3.3V power supply
- ✓ RoHS-2 compliant

Applications

- ✓ Data Center Interconnect



Product Selection

Part Number	Operating Case temperature	DDMI
APQD31HCDMD4A	Commercial(0~70c)	Yes

Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883 Method 3015
- Immunity compatible with EN 61000-4-3
- EMI compatible with FCC Part 15 Class B
- Laser Eye Safety compatible with FDA 21CFR 1040.10 and 1040.11 IEC 60950,IEC60825-1,2

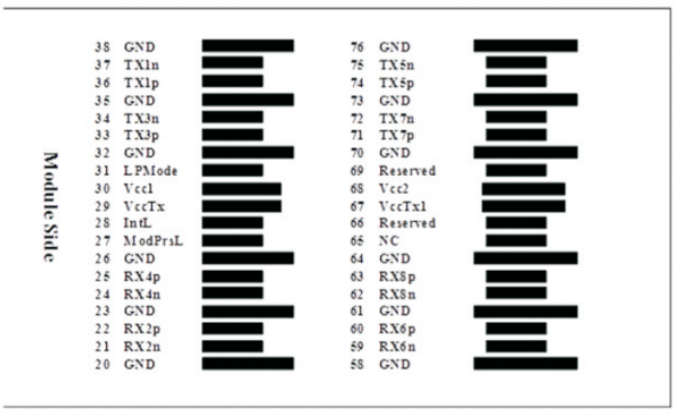
Pin Descriptions

Pin	Logic	Symbol	Description	Plug	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6		Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+ 3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-I	Mod-PrsL	Module Present	3B	
28	LVTTL-I	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	Init-Mode	Initialization mode, In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1

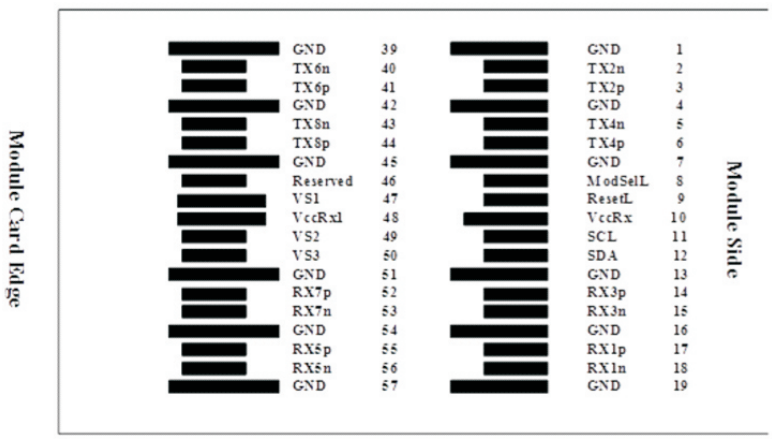
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		Vs1	Module Vendor Specific 1	3A	3
48		VccRx1	+3.3V Power supply	2A	2
49		Vs2	Module Vendor Specific 2	3A	3
50		Vs3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Non-Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Non-Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For Future Use	3A	3
67		VccTx1	+3.3V Power supply	2A	2
68		Vcc2	+3.3V Power supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.
4. Plug Sequence specifies the mating sequence of the host connector and module.

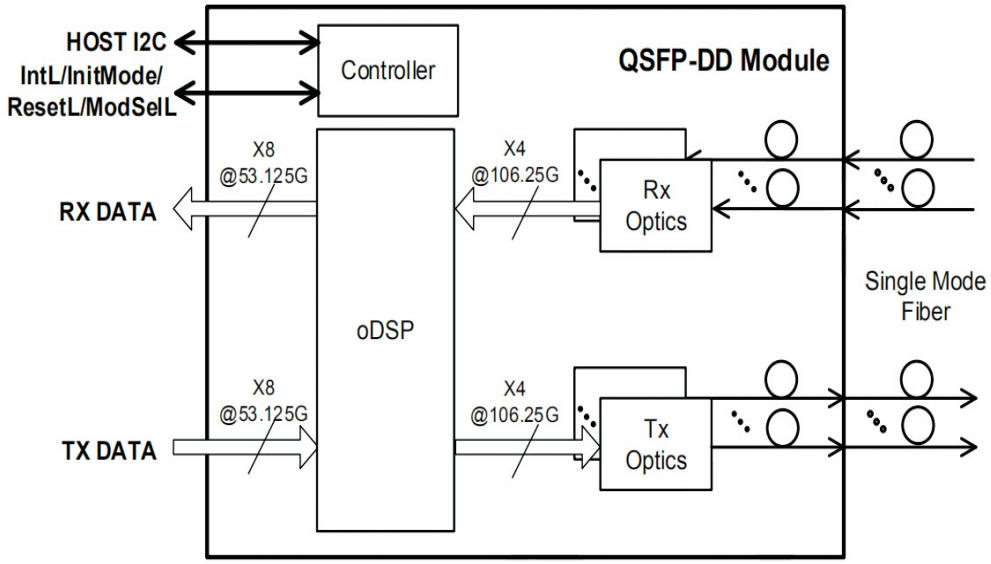


Top Side Viewed from Top



Bottom Side Viewed from Bottom

Transceiver Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.3		+3.6	V	
Storage Temperature	TS	-40		+85	℃	
Operating Humidity	RH	0		85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Supply Voltage	Vcc	3.135	3.30	3.465	V	
Supply Current	Icc			3.63	A	
Case Operating Temperature	Tc	0		+70	℃	Commercial
Power dissipation	P			12	w	
9/125um G.652 SMF	Lmax	2		500	m	
Data Rate Accuracy		-100		100	ppm	

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Receiver(module input)						
Data Rate, each lane			26.5625±100ppm		GBd	
Overload Differential Voltage pk-pk		900			mV	
Common Mode Voltage		-350		2850	mV	
Differential Termination Resistance Mismatch				10	%	1
Differential Return Loss				Equation (16-1)	dB	2
Common Mode to Differential Mode Conversion				Equation (16-3)	dB	2
Stressed Input Test		See OIF-CEI-56G-VSR-PAM4 Section 16.3.10.3				
Transmitter(module output)						
Data Rate, each lane			26.5625±100ppm		GBd	
Differential Voltage pk-pk	Vpp			900	mV	
Common Mode Voltage	Vcm	-350		2850	mV	
Common Mode Noise ,RMS	Vrms			17.5	mV	
Differential Termination Resistance Mismatch				10	%	1
Differential Return Loss	SDD22			Equation (16-1)	dB	
Common Mode to Differential Mode Conversion	SCD22			Equation (16-3)	dB	
Common Mode Return Loss	SCC22			-2	dB	3
Transition Time		9.5			ps	
Near-end Eye Width at 10-6 probability	EW6	0.265			UI	
Near-end Eye Height at 10-6 probability	EH6	70			mV	
Far-end Eye Width at 10-6 probability	EW6	0.2			UI	
Far-end Eye Height at 10-6 probability	EH6	30			mV	
Near-end Eye Linearity		0.85				

Notes:

1.At 1 MHz.

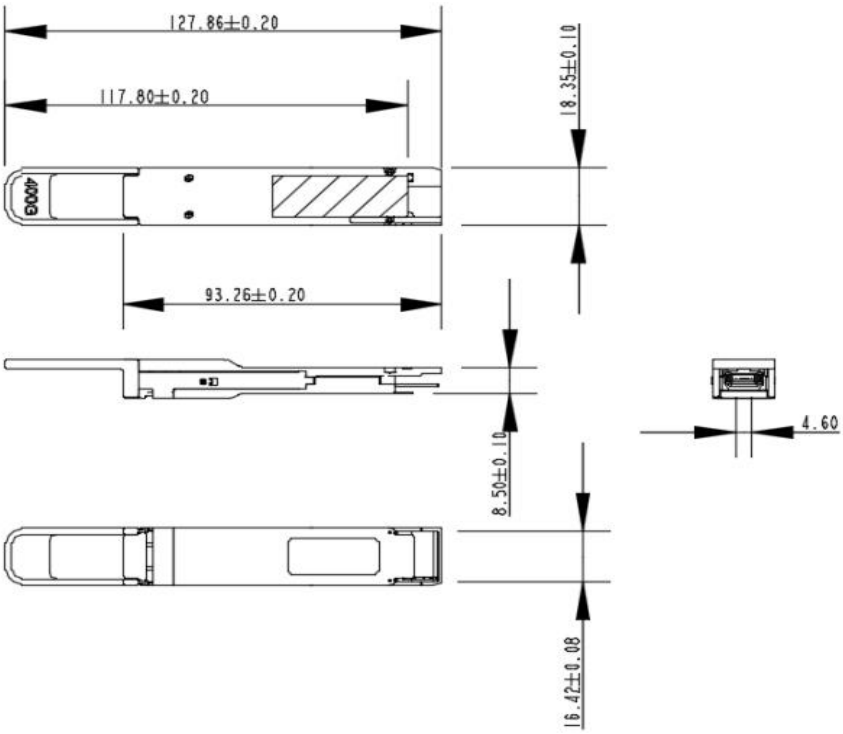
2.OIF-CEI-56G-VSR-PAM4.

3.From 250MHz to fbGHz.

Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Data Rate, each Lane			53.125±100 ppm		GBd	
Modulation Format			PAM4			
Line wavelengths		1304. 5	1311	1317.5	nm	
Average Launch Power, each Lane		-2.9		4	dBm	
Optical Modulation Amplitude(OMA), each Lane		-0.8		4.2	dBm	
Side-mode Suppression Ratio	SMSR	30			dB	
Extinction Ratio	ER	3.5			dB	
Launch power in OMA minus TDECQ, each lane		-2.2			dBm	
Transmitter and Dispersion Eye Clouser for PAM4, each Lane				3.4	dB	
Optical Return Loss Tolerance				21.4	dB	
Transmitter Reflectance				-26	dB	
Average Launch Power of OFF Transmitter, each Lane				-15	dBm	
Receiver						
Data Rate, each Lane			53.125±100ppm		GBd	
Modulation Format			PAM4			
Damage Threshold, each lane		5			dBm	
Line wavelengths		1304. 5		1317. 5	nm	
Average receiver power, each lane		-5.9		4	dBm	
Receiver power, each lane(OMA)				4.2	dBm	
Receiver Sensitivity (OMAouter) each lane (max)				-4.4	dBm	
Stressed receiver Sensitivity (OMAouter), each lane (max)				-1.9	dBm	
LOS De-Assert	LOSD			-8.4	dBm	
LOS Assert	LOSA	-15			dBm	
LOS Hysteresis		0.5			dB	
Conditions of Stressed Receiver Sensitivity						
Stressed eye closure for PAM4 (SECQ), lane under test		0.9		3.4	dB	
OMAouter of each aggressor lane				4.2	dBm	

Mechanical Specifications



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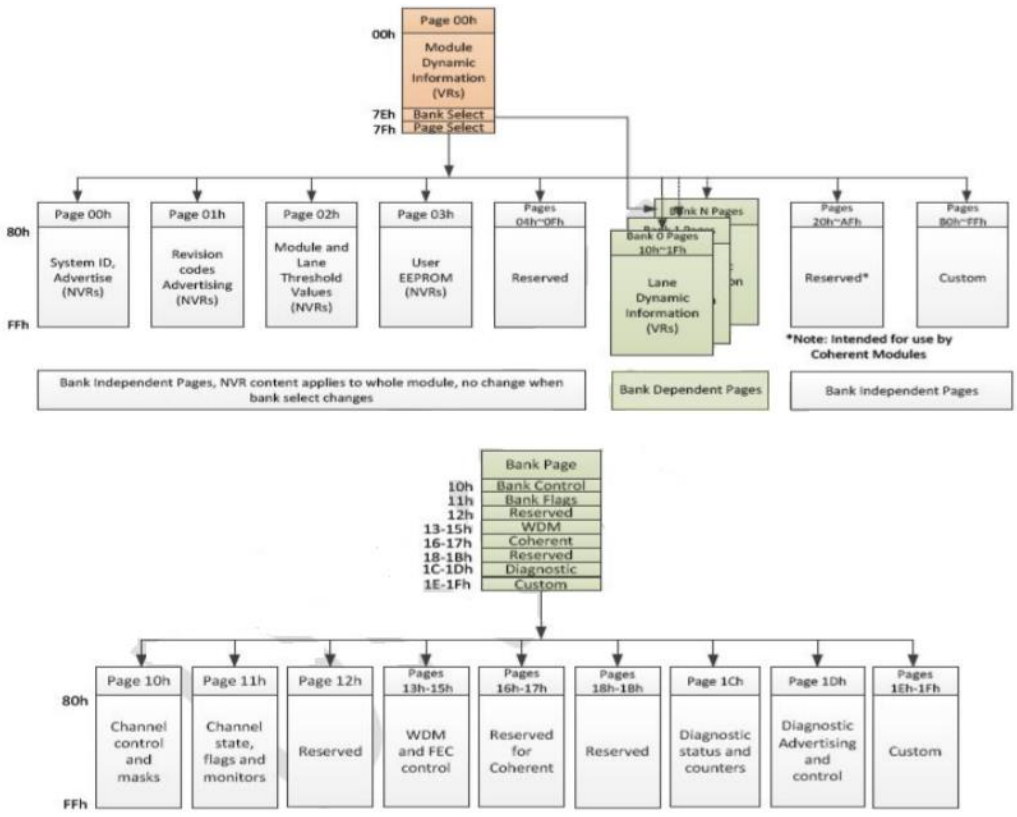
EEPROM Information



Digital Diagnostic Monitoring Interface

Five transceiver parameter values are monitored.

Parameter	Data Address		
	Alarm & Warning	Alarm & Warning Thresholds	Monitor
Temperature	Lowpage 9	Page2h (128-135)	Lowpage (14-15)
Voltage	Lowpage 9	Page2h (136-143)	Lowpage (16-17)
Bias Current	Page11h (143-146)	Page2h (184-191)	Page11h(170-177)
TX Power	Page11h (139-142)	Page2h (176-183)	Page11h(154-161)
RX Power	Page11h (149-152)	Page2h (192-199)	Page11h(186-193)

Revision History

Revision	Initiated	Reviewed	Approved	DCN	Release Date
Version1.0	Billy Tang	Xuming Di	Dingzheng	New Released.	Apr 21, 2019
Version1.1	Tang Rong	Xuming Di	Dingzheng	1.Update the new template. 2.Update the product picture. 3.Update some parameter metrics.	Apr 25, 2021

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