



QSFP28 Passive High-Speed Cable

APCP10-PPCxxx-yy



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The cables are compliant with InfiniBand Architecture, SFF-8636 specifications and provide connectivity between devices using QSFP28 ports. The QSFP28 cable is an assembly of 4 full-duplex lanes, where each lane is capable of transmitting data at rates up to 25Gb/s per direction, providing an aggregated rate of 100Gb/s

Product Features

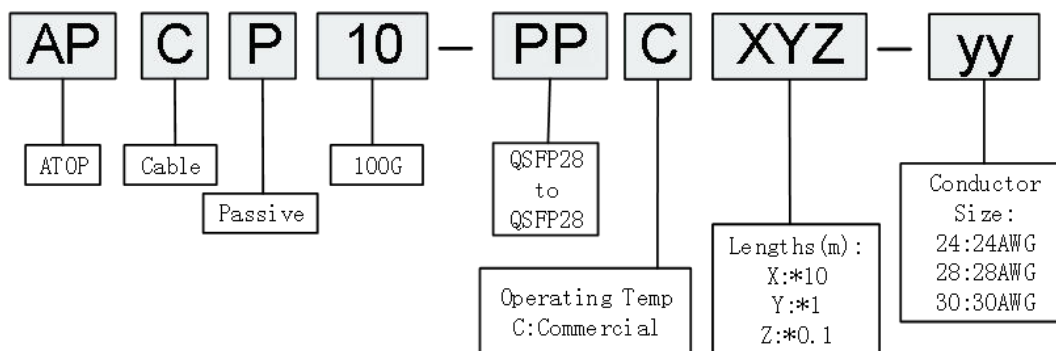
- ✓ Compliant with SFF-8636
- ✓ Compliant with IEEE802.3bj
- ✓ Support 0.5~5m distance
- ✓ All-metal housing for superior EMI performance
- ✓ Low crosstalk
- ✓ Low power consumption
- ✓ RoHS compliant

Applications

- ✓ Data/Servers/ Routers
- ✓ Networked storage systems
- ✓ External storage systems
- ✓ Data Center networking
- ✓ Communications Switches
- ✓ InfiniBand SDR, DDR, QDR, FDR,EDR



Product Selection



Part Number	Lengths	Conductor Size	Note
APCP10-PPC005-yy	0.5m	26/28/30 AWG	1
APCP10-PPC010-yy	1m	26/28/30 AWG	1
APCP10-PPC015-yy	1.5m	26/28/30 AWG	1
APCP10-PPC020-yy	2m	26/28/30 AWG	1
APCP10-PPC025-yy	2.5m	26/28/30 AWG	1
APCP10-PPC030-yy	3m	26/28/30 AWG	1
APCP10-PPC050-yy	5m	26/28/30 AWG	1

Note:

1, yy=30,28,26, present wire size AWG

Pin Descriptions

Pin	Symbol	Name	Ref.
1	GND	Ground	
2	Tx2n	Transmitter Inverted Data Input, CML-I	
3	Tx2p	Transmitter Non-Inverted Data output, CML-I	
4	GND	Ground	
5	Tx4n	Transmitter Inverted Data Input, CML-I	
6	Tx4p	Transmitter Non-Inverted Data output, CML-I	
7	GND	GND	
8	ModSelL	<p>The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node must be biased to the "High" state in the module</p>	
9	ResetL	<p>The ResetL pin must be pulled to Vcc in the QSFP+ module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released.</p>	
10	VccRx	+ 3.3V Power Supply Receiver	
11	SCL	2-Wire Serial Interface Clock	
12	SDA	2-Wire Serial Interface Data	
13	GND	GND	
14	Rx3p	Receiver Non-Inverted Data Output, CML-O	
15	Rx3n	Receiver Inverted Data Output, CML-O	

Signal Integrity

ITEM	REQUIREMENT	TEST CONDITION																																			
Cable Impedance	105+5/-10Ω																																				
Differential Impedance	Paddle Card Impedance 100±10Ω	Rise time of 25ps (20 % - 80 %).																																			
	Cable Termination Impedance 100±15Ω																																				
[Differential (Input/Output) Return loss SDD11/SDD22]	$\text{Return_loss}(f) \geq \begin{cases} 16.5-2\sqrt{f} & 0.05 \leq f < 4.1 \\ 10.66-14\log_{10}(f/5.5) & 4.1 \leq f \leq 19 \end{cases}$ <p>Where f is the frequency in GHz Return_loss(f) is the return loss at frequency f</p>	10MHz ≤ f ≤ 19GHz																																			
[Differential to common-mode (Input/Output)Return loss SCD11/SCD22]	$\text{Return_loss}(f) \geq \begin{cases} 22-(20/25.78)f & 0.01 \leq f < 12.89 \\ 15-(6/25.78)f & 12.89 \leq f \leq 19 \end{cases}$ <p>Where f is the frequency in GHz Return_loss(f) is the Differential to common-mode return loss at frequency f</p>	10MHz ≤ f ≤ 19GHz																																			
Common-mode to Common-mode(Input/Output)Return loss SCC11/SCC22	$\text{Return_loss}(f) \geq 2\text{dB} \quad 0.2 \leq f \leq 19$ <p>Where f is the frequency in GHz Return_loss(f) is the common-mode to common-mode return loss at frequency f</p>	10MHz ≤ f ≤ 19GHz																																			
(Differential Insertion Loss Max. For TPa to TPb Excluding Test fixture)																																					
Differential Insertion Loss (SDD21 Max.)	<table border="1"> <thead> <tr> <th>AWG \ F</th> <th>1.25GHz</th> <th>2.5GHz</th> <th>5.0GHz</th> <th>7.0GHz</th> <th>10GHz</th> <th>12.89GHz</th> </tr> </thead> <tbody> <tr> <td>30(1m)Max.</td> <td>4.5dB</td> <td>5.4dB</td> <td>6.3dB</td> <td>7.5dB</td> <td>8.5dB</td> <td>10.5dB</td> </tr> <tr> <td>30/28(3m)Max.</td> <td>7.5dB</td> <td>9.5dB</td> <td>12.2dB</td> <td>14.8dB</td> <td>18.0dB</td> <td>21.5dB</td> </tr> <tr> <td>26(3m)Max.</td> <td>5.7dB</td> <td>7.2dB</td> <td>9.9dB</td> <td>11.9dB</td> <td>14.1dB</td> <td>16.5dB</td> </tr> <tr> <td>26/25(5m)Max.</td> <td>7.8dB</td> <td>10.0dB</td> <td>13.5dB</td> <td>16.0dB</td> <td>19.0dB</td> <td>22.0dB</td> </tr> </tbody> </table>	AWG \ F	1.25GHz	2.5GHz	5.0GHz	7.0GHz	10GHz	12.89GHz	30(1m)Max.	4.5dB	5.4dB	6.3dB	7.5dB	8.5dB	10.5dB	30/28(3m)Max.	7.5dB	9.5dB	12.2dB	14.8dB	18.0dB	21.5dB	26(3m)Max.	5.7dB	7.2dB	9.9dB	11.9dB	14.1dB	16.5dB	26/25(5m)Max.	7.8dB	10.0dB	13.5dB	16.0dB	19.0dB	22.0dB	10MHz ≤ f ≤ 19GHz
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Insertion Loss Deviation	$-0.176*f - 0.7 \leq \text{ILD} \leq 0.176*f + 0.7$	50MHz ≤ f ≤ 19GHz																																			
Differential to common-mode Conversion Loss-Differential Insertion Loss(SCD21-SDD21)	$\text{Conversion_loss}(f) - \text{IL}(f) \geq \begin{cases} 10 & 0.01 \leq f < 12.89 \\ 27-(29/22)f & 12.89 \leq f < 15.7 \\ 6.3 & 15.7 \leq f \leq 19 \end{cases}$ <p>Where f is the frequency in GHz Conversion_loss(f) is the cable assembly differential to common-mode conversion loss IL(f) is the cable assembly insertion loss</p>	10MHz ≤ f ≤ 19GHz																																			
MDNEXT(multiple disturber near-end crosstalk)	≥35dB @12.89GHz	10MHz ≤ f ≤ 19GHz																																			
Intra Skew	15ps/m	10MHz ≤ f ≤ 19GHz																																			

Other Electrical Performance

ITEM	REQUIREMENT	TEST CONDITION
Low Level Contact Resistance	70milliohms Max. From initial.	EIA-364-23:Apply a maximum voltage of 20mV And a current of 100 mA.
Insulation Resistance	10Mohm(Min.)	EIA364-21:AC 300V 1 minute
Dielectric Withstanding Voltage	NO disruptive discharge.	EIA-364-20:Apply a voltageof 300VDC for 1 minute between adjacent terminals And between adjacent terminals and ground.

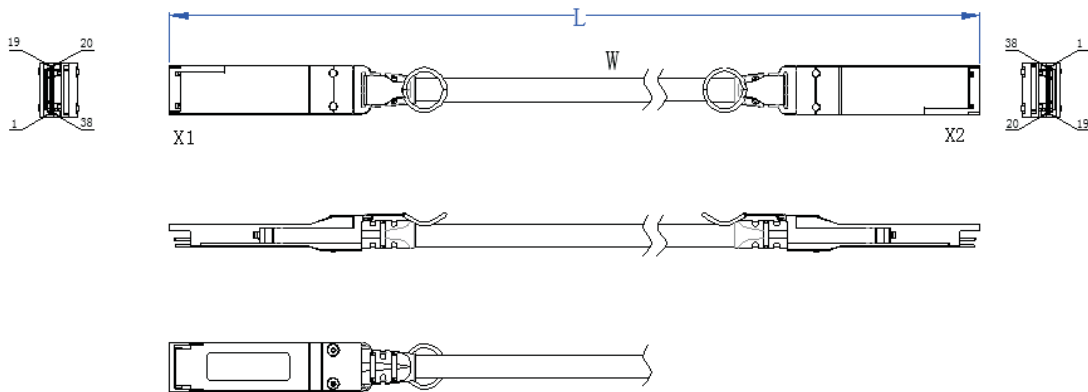
Environment Performance

ITEM	REQUIREMENT	TEST CONDITION
Operating Temp. Range	0°C to +70°C	Cable operating temperature range.
Storage Temp. Range (in packed condition)	-40°C to +80°C	Cable storage temperature range in packed condition.
Thermal Cycling Non-Powered	No evidence of physical damage	EIA-364-32D, Method A, -25 to 90C, 100 cycles, 15 min. dwells
Salt Spraying	48 hours salt spraying after shell corrosive area less than 5%.	EIA-364-26
Mixed Flowing Gas	Pass electrical tests per 3.1 after stressing. (For connector only)	EIA-364-35 Class II, 14 days.
Temp. Life	No evidence of physical damage	EIA-364-17C w/ RH, Damp heat 90°C at 85% RH for 500 hours then return to ambient
Cable Cold Bend	4H, No evidence of physical damage	Condition: -20°C ±2°C , mandrel diameter is 6 times the cable diameter.

Mechanical and Physical Characteristics

ITEM	REQUIREMENT	TEST CONDITION
Vibration	Pass electrical tests per 3.1 after stressing.	Clamp & vibrate per EIA-364-28E,TC-VII, test condition letter – D, 15 minutes in X, Y & Z axis.
Cable Flex	No evidence of physical damage	Flex cable 180° for 20 cycles ($\pm 90^\circ$ from nominal position) at 12 cycles per minute with a 1.0kg load applied to the cable jacket. Flex in the boot area 90° in each direction from vertical. Per EIA-364-41C
Cable Plug Retention in Cage	90N Min. No evidence of physical damage	Pull on cable jacket approximately 1 ft behind cable plug. No functional damage to cable plug below 90N. Per SFF-8432 Rev 5.0
Cable Retention in Plug	90N Min. No evidence of physical damage	Cable plug is fixtured with the bulk cable hanging vertically. A 90N axial load is applied (gradually) to the cable jacket and held for 1 minute. Per EIA-364-38B
Mechanical Shock	Pass electrical tests Per 3.1 after stressing.	Clamp and shock per EIA-364-27B, TC-G,3 times in 6 directions, 100g, 6ms.
Cable Plug Insertion	40N Max	Per SFF-8436 Rev 5.4.1.
Cable plug Extraction	30N Max	Place axial load on de-latch to de-latch plug. Per SFF-8436 Rev 5.4.1.
Durability	50 cycles, No evidence of physical damage	EIA-364-09, perform plug & unplug cycles: Plug and receptacle mate rate: 250times/hour. 50times for module (CONNECTOR TO PCB)

Mechanical Specifications

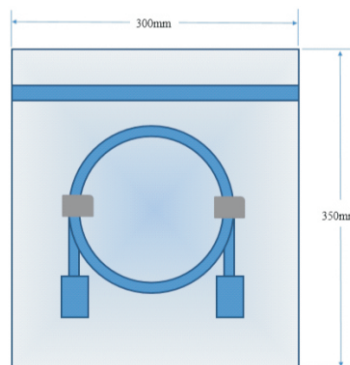


Wiring Diagram

X1	X2	REMARKS	X1	X2	REMARKS
18(RX1-)	37(TX1-)	pair	37(TX1-)	18(RX1-)	pair
17(RX1+)	36(TX1+)		36(TX1+)	17(RX1+)	
15(RX3-)	34(TX3-)	pair	34(TX3-)	15(RX3-)	pair
14(RX3+)	33(TX3+)		33(TX3+)	14(RX3+)	
6 (TX4+)	25(RX4+)	pair	25(RX4+)	6 (TX4+)	pair
5 (TX4-)	24(RX4-)		24(RX4-)	5 (TX4-)	
3 (TX2+)	22(RX2+)	pair	22(RX2+)	3 (TX2+)	pair
2 (TX2-)	21(RX2-)		21(RX2-)	2 (TX2-)	
1, 4, 7, 13, 16, 19, 20, 23, 26, 32, 35, 38	1, 4, 7, 13, 16, 19, 20, 23, 26, 32, 35, 38	GND	8, 9, 10, 11, 12, 27, 28, 29, 30, 31	8, 9, 10, 11, 12, 27, 28, 29, 30, 31	EEPROM point at both ends

Package diagram

<=2m: 200mm*300mm
>2m: 300mm*350mm



Revision History

Revision	Initiated	Reviewed	Approved	DCN	Release Date
Version1.0	Tangzhiqiang	Li Tao	Ding zheng	New Released.	Nov 19, 2019



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